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a second buried impurity region of a second conductive type formed between said first buried impurity region and said semiconductor layer;

*B*  
*Cont*

a first impurity region of the second conductive type which is formed in the surface of said semiconductor layer and which is electrically connected to said second buried impurity region;

a second impurity region of the first conductive type which is formed in the surface or inside of said semiconductor layer located in a region above said second buried impurity region; and

a semiconductor element which includes said first impurity region and said second impurity region and which has a switching function formed on the surface of said semiconductor layer,

wherein the withstanding voltage is secured by a depletion layer extending from an interface between said second buried impurity region and said semiconductor layer under the condition where said semiconductor element is turned OFF; and

said second buried impurity region includes a first gap part wherein said second buried impurity region is disconnected, said gap part of the second buried impurity region positioned directly beneath said second impurity region.

*BB*

10. (Amended) A semiconductor device including:

a semiconductor substrate having a main surface;

a semiconductor layer of a first conductive type formed on the main surface of said semiconductor substrate;

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a buried impurity region of the first conductive type formed between said semiconductor substrate and said semiconductor layer;

*B2  
cont.*  
a first impurity region of the first conductive type which is formed on the surface of said semiconductor layer and which is electrically connected to said buried impurity region;

a second impurity region of a second conductive type formed on a surface of said semiconductor layer located in a region above said buried impurity region; and

a semiconductor element which includes said first impurity region and said second impurity region and which has a switching function formed on the surface of said semiconductor layer,

wherein a withstanding voltage is secured by a depletion layer extending from an interface between said second impurity region and said semiconductor layer under the condition where said semiconductor element is turned off; and

said buried impurity region includes a gap part wherein said buried region is disconnected, said gap part of the second buried impurity region positioned directly beneath said second impurity region.

#### REMARKS

At the time of the Office Action dated June 4, 2002, claims 1-13 were pending and rejected in this application. Claims 1 and 10 have been amended, and care has been exercised to avoid the introduction of new matter. Specifically, claims 1 and 10 have been amended to recite that a gap part is positioned directly beneath a second impurity region. Support for this limitation can be found throughout the originally filed disclosure, for example, on page 12, lines 20-23. Applicant submits that the present Amendment does not generate any new matter issue.